IN THE CLAIMS

A listing of all claims and their current status in accordance with 37 C.F.R. § 1.121(c) is provided below.

1-34. (Canceled)

35. (Previously Presented) An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature.

36. (Canceled)

37. (Previously Presented) The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

38. (Previously Presented) An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack.

39. (Previously Presented) The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die.

40-67. (Canceled)

68. (Previously Presented) An integrated circuit comprising:

a stack comprising at least two semiconductor die, each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature; and

a substrate coupled to one of the at least two semiconductor die by a second adhesive, the second adhesive being curable at a second temperature lower than the first temperature;

wherein each die in the stack of at least two die is successively thinner than the previous die as the die approach the substrate.

69-70. (Canceled)

71. (Previously Presented) An integrated circuit comprising:

a stack of at least two semiconductor die, each of the die being coupled to an adjacent die in the stack by a respective layer of a first adhesive prior to the stack being coupled to a packaging substrate, wherein the first adhesive is curable at a first temperature; and

a second adhesive disposed on an outer side of the stack to facilitate coupling the stack with the packaging substrate, wherein the second adhesive is curable at a second temperature lower than the first temperature.

72. (Previously Presented) The integrated circuit, as set forth in claim 71, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die.

73. (Previously Presented) The integrated circuit, as set forth in claim 71, wherein at least one of the at least two semiconductor die comprises a memory die.

74. (Previously Presented) An integrated circuit package comprising:

a substrate; and

a die stack coupled to the substrate, wherein the die stack comprises at least two semiconductor die coupled together via a first adhesive that is curable at a first temperature and has been cured; and

a second adhesive disposed between the die stack and the substrate that is curable at a second temperature lower than the first temperature.

75. (Previously Presented) The integrated circuit package, as set forth in claim 74, wherein at least one of the at least two semiconductor die comprises a memory die.